FIG. 1

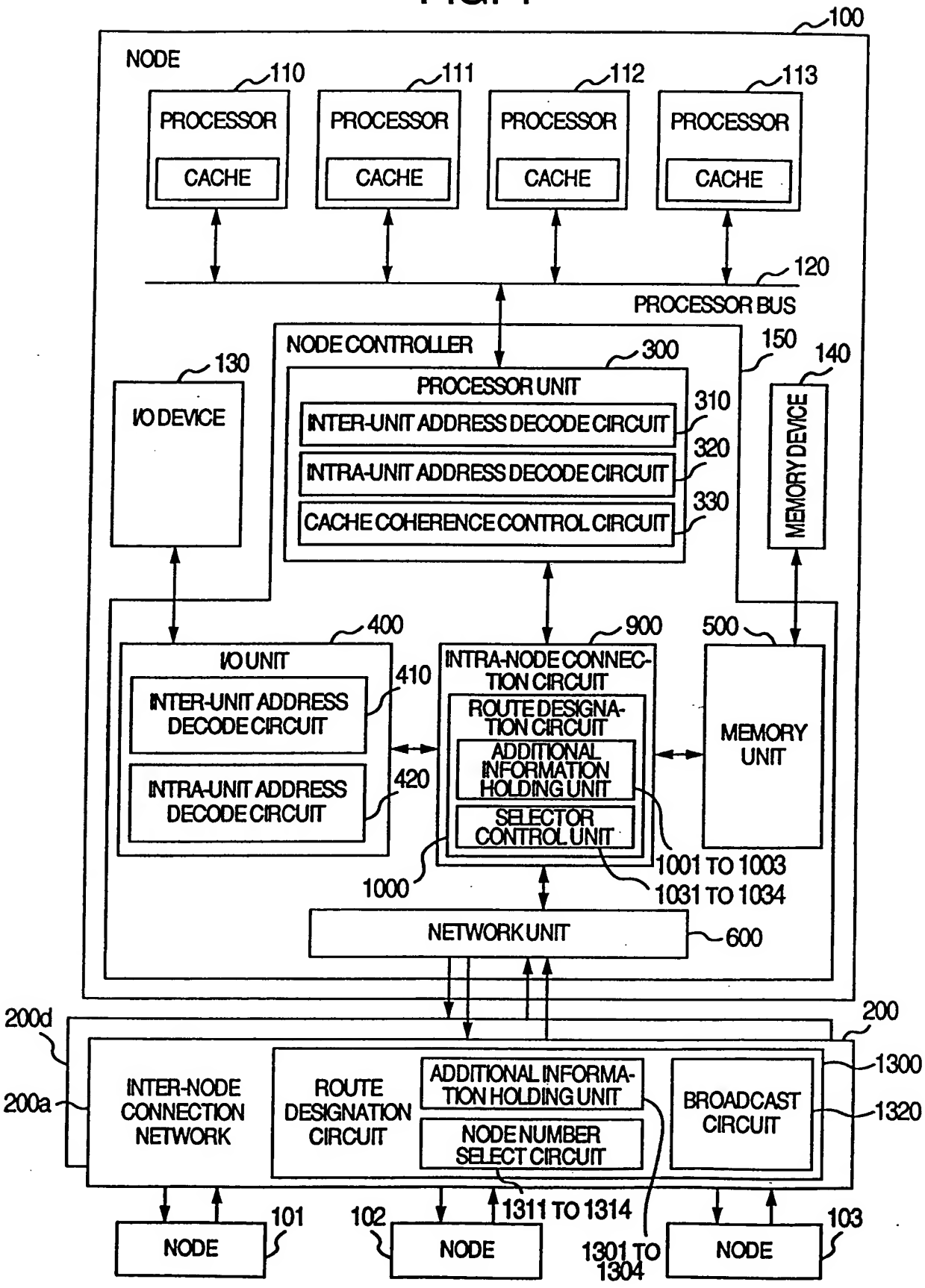

100
NODE
110
111
112
113
PROCESSOR
CACHE
120
PROCESSOR BUS
NODE CONTROLLER
300
150
140
130
I/O DEVICE
PROCESSOR UNIT
310
INTER-UNIT ADDRESS DECODE CIRCUIT
320
INTRA-UNIT ADDRESS DECODE CIRCUIT
330
CACHE COHERENCE CONTROL CIRCUIT
MEMORY DEVICE
400
900
500
I/O UNIT
410
INTER-UNIT ADDRESS DECODE CIRCUIT
420
INTRA-UNIT ADDRESS DECODE CIRCUIT
INTRA-NODE CONNEC-TION CIRCUIT
ROUTE DESIGNA-TION CIRCUIT
ADDITIONAL INFORMATION HOLDING UNIT
SELECTOR CONTROL UNIT
MEMORY UNIT
1000
1001 TO 1003
1031 TO 1034
NETWORK UNIT
600
200d
200
200a
INTER-NODE CONNECTION NETWORK
ROUTE DESIGNATION CIRCUIT
ADDITIONAL INFORMA-TION HOLDING UNIT
NODE NUMBER SELECT CIRCUIT
1300
BROADCAST CIRCUIT
1320
1311 TO 1314
101
102
103
NODE
NODE
NODE
1301 TO 1304

FIG. 2

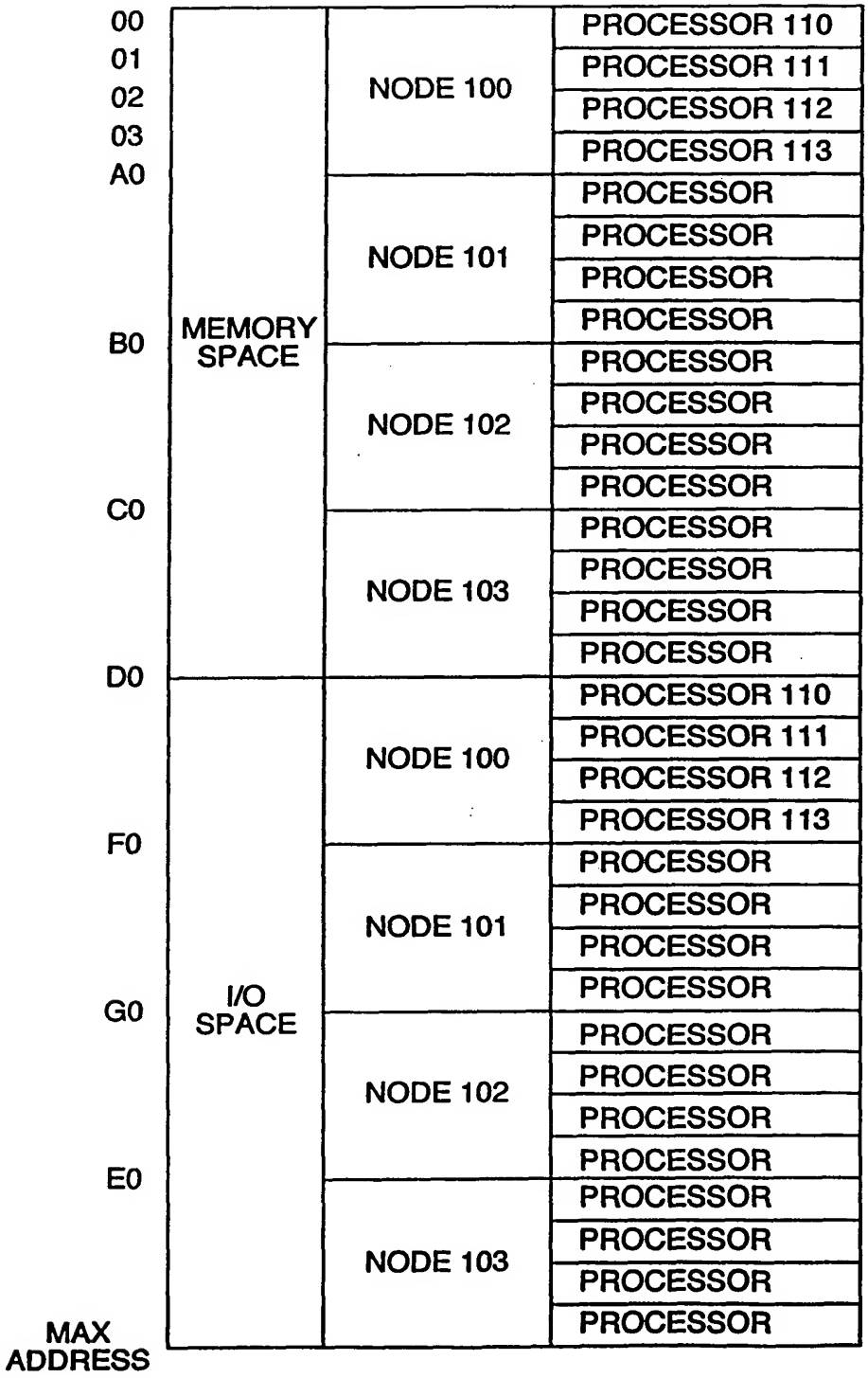

00
01
02
03
A0
B0
C0
D0
F0
G0
E0
MAX ADDRESS
MEMORY SPACE
I/O SPACE
NODE 100
NODE 101
NODE 102
NODE 103
PROCESSOR 110
PROCESSOR 111
PROCESSOR 112
PROCESSOR 113
PROCESSOR

FIG. 3A

FIG. 3B

FIG. 3C

TYPE OF ACCESS REQUEST	Tx INFORMATION
READ REQUEST REQUIRING CACHE COHERENCE CONTROL	TYPE1
WRITE REQUEST REQUIRING CACHE COHERENCE CONTROL	TYPE2
READ REQUEST NOT REQUIRING CACHE COHERENCE CONTROL	TYPE3
WRITE REQUEST NOT REQUIRING CACHE COHERENCE CONTROL	TYPE4
READ RESPONSE	TYPE5

FIG. 4

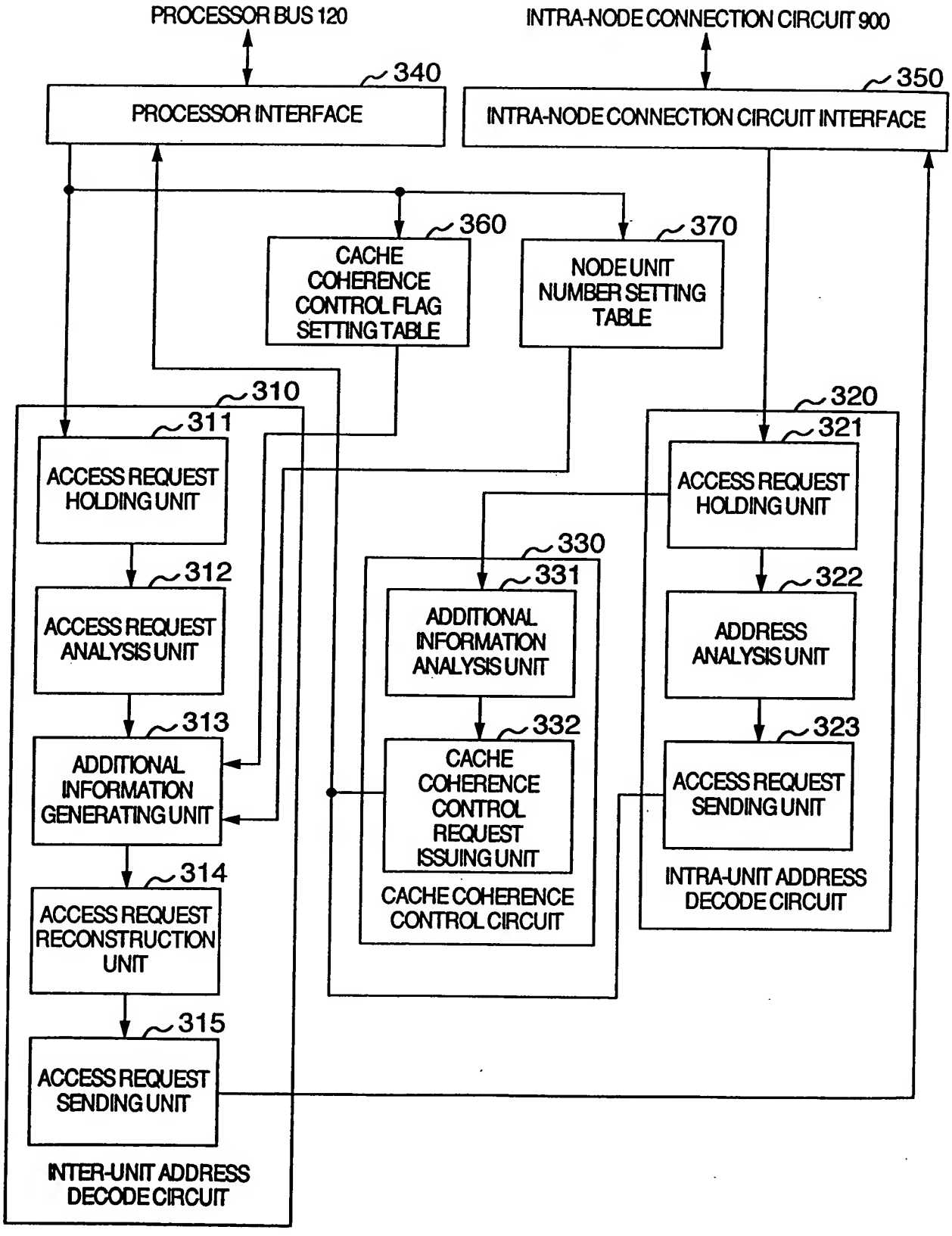

PROCESSOR BUS 120
INTRA-NODE CONNECTION CIRCUIT 900
340
PROCESSOR INTERFACE
350
INTRA-NODE CONNECTION CIRCUIT INTERFACE
360
CACHE COHERENCE CONTROL FLAG SETTING TABLE
370
NODE UNIT NUMBER SETTING TABLE
310
311
ACCESS REQUEST HOLDING UNIT
312
ACCESS REQUEST ANALYSIS UNIT
313
ADDITIONAL INFORMATION GENERATING UNIT
314
ACCESS REQUEST RECONSTRUCTION UNIT
315
ACCESS REQUEST SENDING UNIT
INTER-UNIT ADDRESS DECODE CIRCUIT
330
331
ADDITIONAL INFORMATION ANALYSIS UNIT
332
CACHE COHERENCE CONTROL REQUEST ISSUING UNIT
CACHE COHERENCE CONTROL CIRCUIT
320
321
ACCESS REQUEST HOLDING UNIT
322
ADDRESS ANALYSIS UNIT
323
ACCESS REQUEST SENDING UNIT
INTRA-UNIT ADDRESS DECODE CIRCUIT

FIG. 5

360

Tx INFORMATION	CACHE COHERENCE CONTROL FLAG
TYPE1	1
TYPE2	1
TYPE3	0
TYPE4	0
TYPE5	0

FIG. 6

370

ADDRESS RANGE		NODE NO.	UNIT NO.	NODE INDICATED BY NODE NO.	UNIT INDICATED BY UNIT NO.
MINIMUM	MAXIMUM				
00	A0	0	1	100	500
A0	B0	1	1	101	500
B0	C0	2	1	102	500
C0	D0	3	1	103	500
D0	E0	0	2	100	400
E0	F0	1	2	101	400
F0	G0	2	2	102	400
G0	MAX	3	2	103	400

FIG. 7

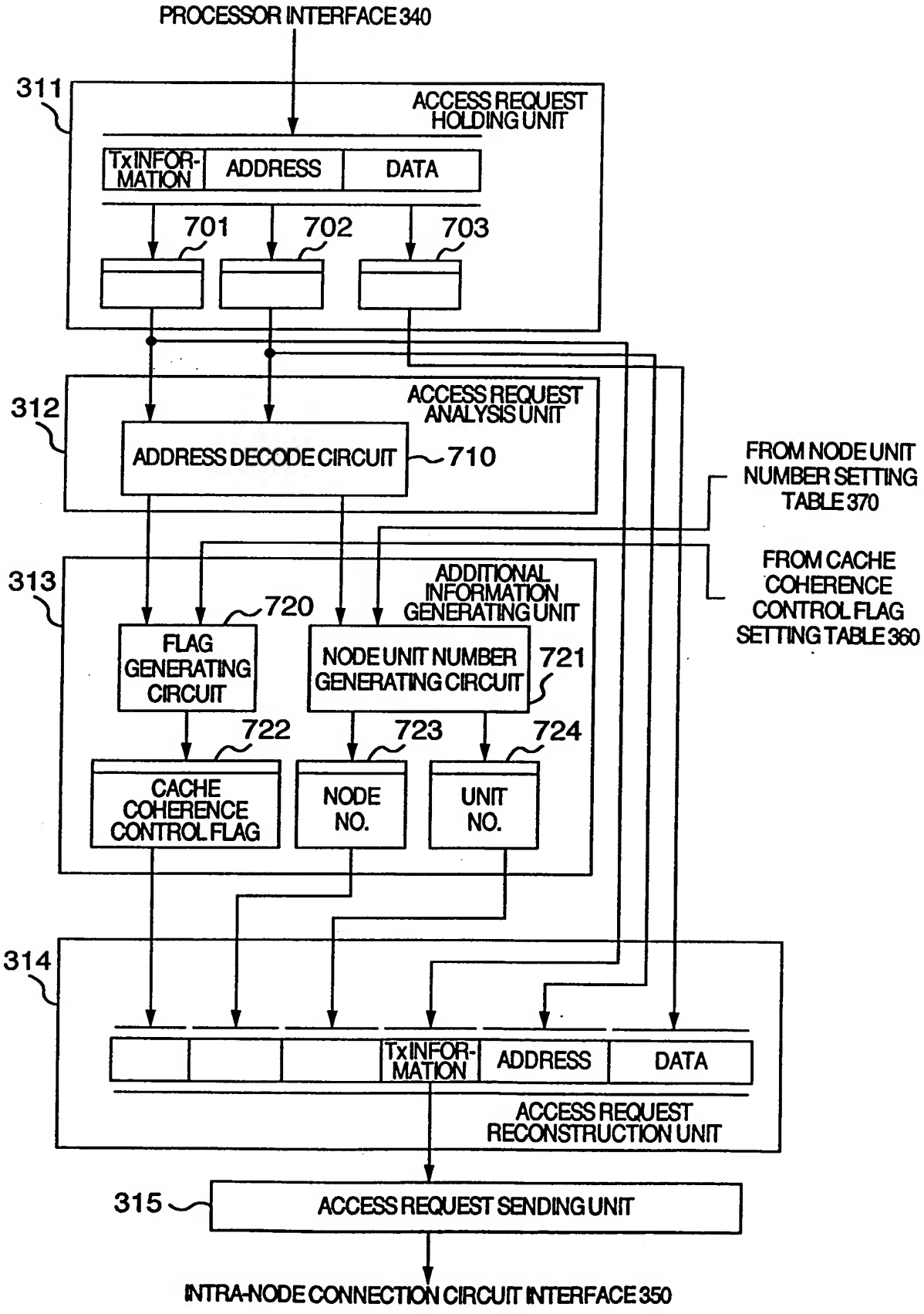

PROCESSOR INTERFACE 340
311
ACCESS REQUEST HOLDING UNIT
TxINFOR-MATION
ADDRESS
DATA
701
702
703
312
ACCESS REQUEST ANALYSIS UNIT
ADDRESS DECODE CIRCUIT
710
FROM NODE UNIT NUMBER SETTING TABLE 370
FROM CACHE COHERENCE CONTROL FLAG SETTING TABLE 360
313
ADDITIONAL INFORMATION GENERATING UNIT
720
FLAG GENERATING CIRCUIT
NODE UNIT NUMBER GENERATING CIRCUIT
721
722
723
724
CACHE COHERENCE CONTROL FLAG
NODE NO.
UNIT NO.
314
TxINFOR-MATION
ADDRESS
DATA
ACCESS REQUEST RECONSTRUCTION UNIT
315
ACCESS REQUEST SENDING UNIT
INTRA-NODE CONNECTION CIRCUIT INTERFACE 350

FIG. 8

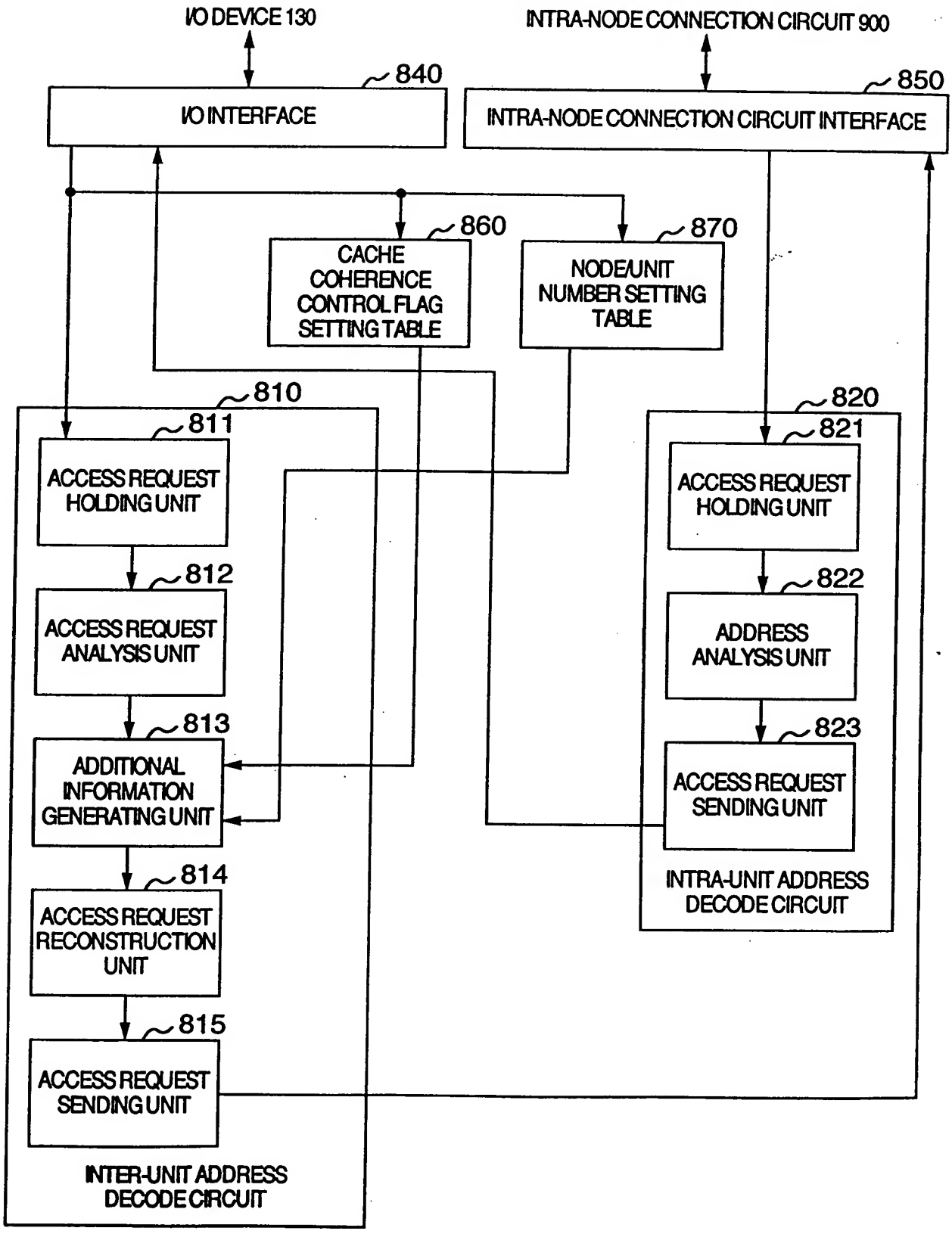

I/O DEVICE 130
INTRA-NODE CONNECTION CIRCUIT 900
840
I/O INTERFACE
850
INTRA-NODE CONNECTION CIRCUIT INTERFACE
860
CACHE COHERENCE CONTROL FLAG SETTING TABLE
870
NODE/UNIT NUMBER SETTING TABLE
810
811
ACCESS REQUEST HOLDING UNIT
812
ACCESS REQUEST ANALYSIS UNIT
813
ADDITIONAL INFORMATION GENERATING UNIT
814
ACCESS REQUEST RECONSTRUCTION UNIT
815
ACCESS REQUEST SENDING UNIT
INTER-UNIT ADDRESS DECODE CIRCUIT
820
821
ACCESS REQUEST HOLDING UNIT
822
ADDRESS ANALYSIS UNIT
823
ACCESS REQUEST SENDING UNIT
INTRA-UNIT ADDRESS DECODE CIRCUIT

FIG. 9

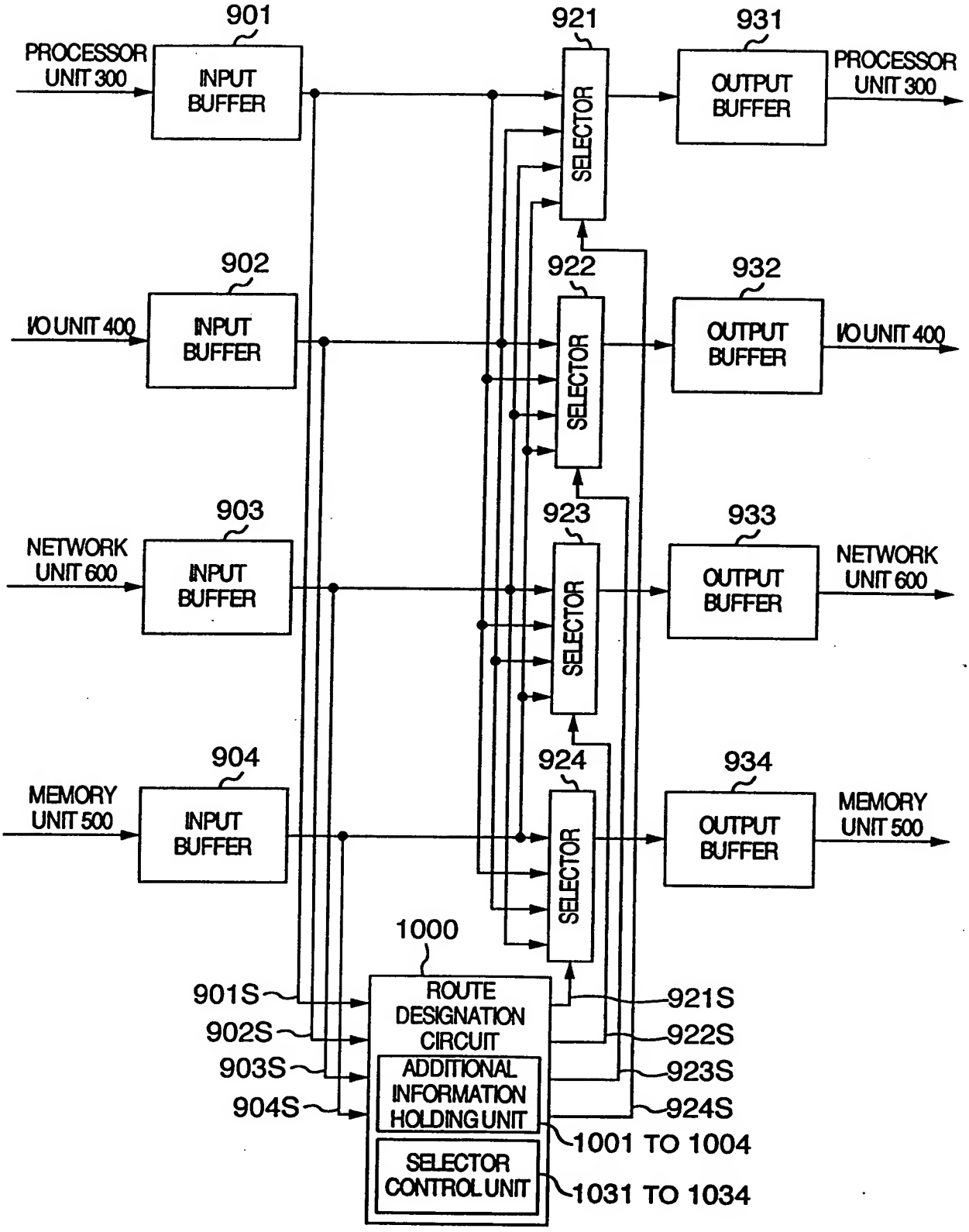

901
921
931
PROCESSOR UNIT 300
INPUT BUFFER
SELECTOR
OUTPUT BUFFER
PROCESSOR UNIT 300
902
922
932
I/O UNIT 400
INPUT BUFFER
SELECTOR
OUTPUT BUFFER
I/O UNIT 400
903
923
933
NETWORK UNIT 600
INPUT BUFFER
SELECTOR
OUTPUT BUFFER
NETWORK UNIT 600
904
924
934
MEMORY UNIT 500
INPUT BUFFER
SELECTOR
OUTPUT BUFFER
MEMORY UNIT 500
1000
901S
902S
903S
904S
ROUTE DESIGNATION CIRCUIT
ADDITIONAL INFORMATION HOLDING UNIT
SELECTOR CONTROL UNIT
921S
922S
923S
924S
1001 TO 1004
1031 TO 1034

FIG. 10

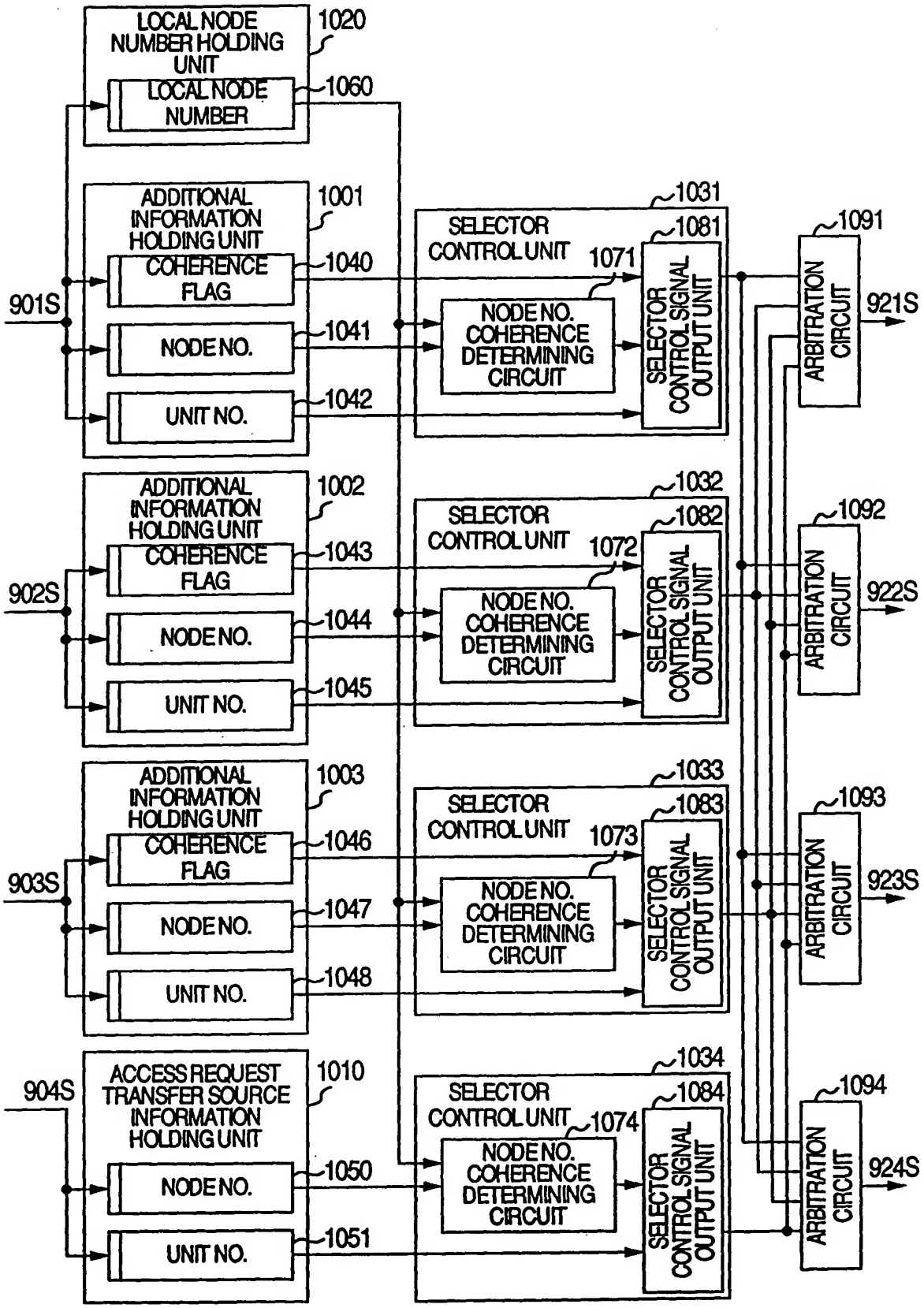

LOCAL NODE NUMBER HOLDING UNIT
1020
LOCAL NODE NUMBER
1060
ADDITIONAL INFORMATION HOLDING UNIT
1001
COHERENCE FLAG
1040
NODE NO.
1041
UNIT NO.
1042
901S
ADDITIONAL INFORMATION HOLDING UNIT
1002
COHERENCE FLAG
1043
NODE NO.
1044
UNIT NO.
1045
902S
ADDITIONAL INFORMATION HOLDING UNIT
1003
COHERENCE FLAG
1046
NODE NO.
1047
UNIT NO.
1048
903S
ACCESS REQUEST TRANSFER SOURCE INFORMATION HOLDING UNIT
1010
NODE NO.
1050
UNIT NO.
1051
904S
SELECTOR CONTROL UNIT
1031
1071
NODE NO. COHERENCE DETERMINING CIRCUIT
1081
SELECTOR CONTROL SIGNAL OUTPUT UNIT
SELECTOR CONTROL UNIT
1032
1072
NODE NO. COHERENCE DETERMINING CIRCUIT
1082
SELECTOR CONTROL SIGNAL OUTPUT UNIT
SELECTOR CONTROL UNIT
1033
1073
NODE NO. COHERENCE DETERMINING CIRCUIT
1083
SELECTOR CONTROL SIGNAL OUTPUT UNIT
SELECTOR CONTROL UNIT
1034
1074
NODE NO. COHERENCE DETERMINING CIRCUIT
1084
SELECTOR CONTROL SIGNAL OUTPUT UNIT
ARBITRATION CIRCUIT
1091
921S
ARBITRATION CIRCUIT
1092
922S
ARBITRATION CIRCUIT
1093
923S
ARBITRATION CIRCUIT
1094
924S

FIG. 11

ACCESS REQUEST TRANSFER SOURCE UNIT	CACHE COHERENCE CONTROL FLAG	OUTPUT OF NODE NO. COHERENCE DETERMINING CIRCUIT	SELECT SIGNAL OUTPUT DESTINATION UNIT
PROCESSOR UNIT	0	0	NETWORK UNIT
	0	1	UNIT NO. DESIGNATION UNIT
	1	0	NETWORK UNIT
	1	1	NETWORK UNIT UNIT NO. DESIGNATION UNIT
I/O UNIT	0	0	NETWORK UNIT
	0	1	UNIT NO. DESIGNATION UNIT
	1	0	NETWORK UNIT
	1	1	NETWORK UNIT UNIT NO. DESIGNATION UNIT
NETWORK UNIT	0	0	NOT OUTPUT
	0	1	UNIT NO. DESIGNATION UNIT
	1	0	PROCESSOR UNIT
	1	1	PROCESSOR UNIT UNIT NO. DESIGNATION UNIT
MEMORY UNIT	*	0	NETWORK UNIT
	*	1	ACCESS REQUEST TRANSFER SOURCE UNIT

FIG. 14

1400

NODE NO.	CACHE COHERENCE CONTROL REQUIRED OR NOT
100	1
101	1
102	0
103	1

FIG. 12

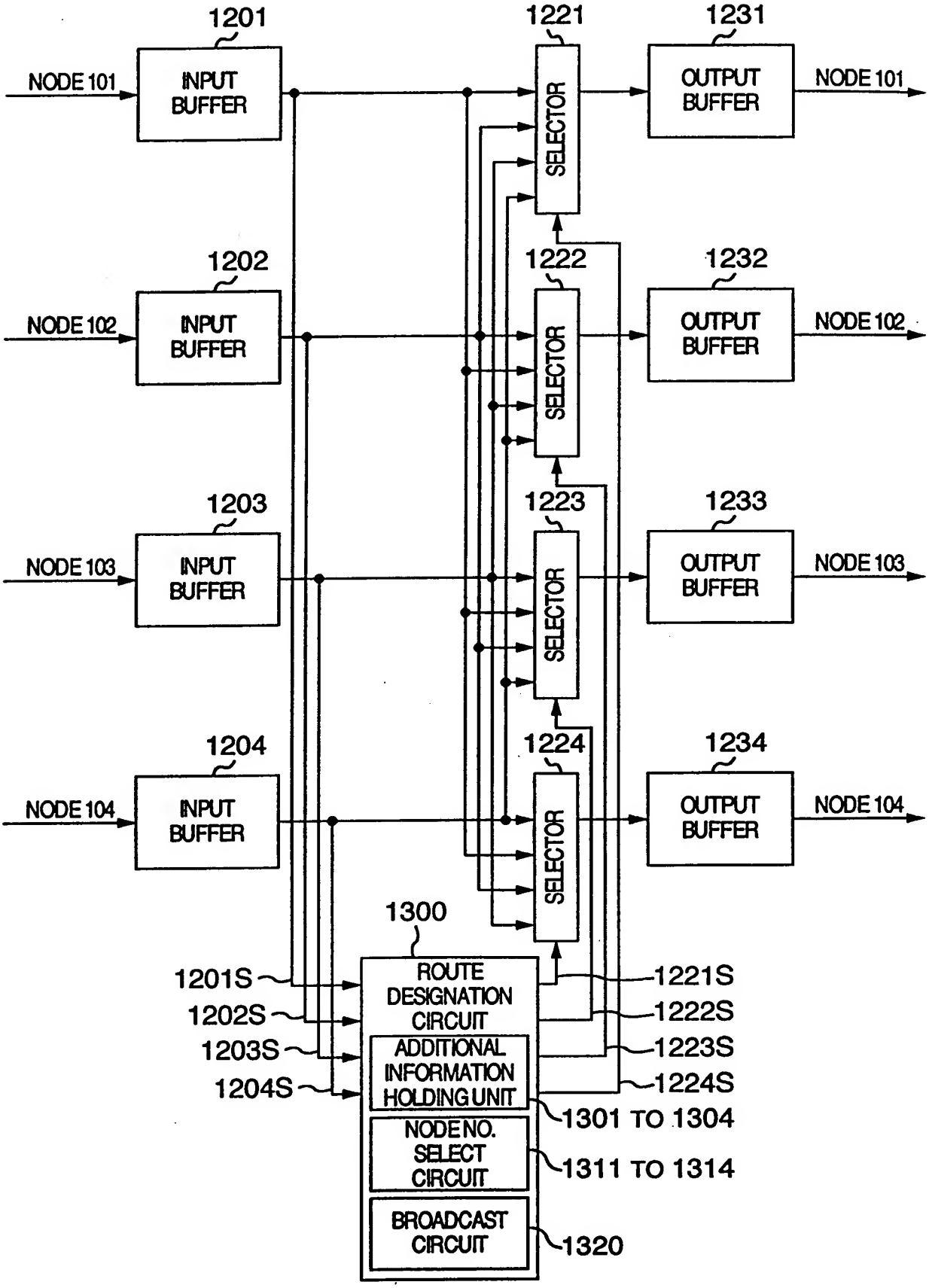
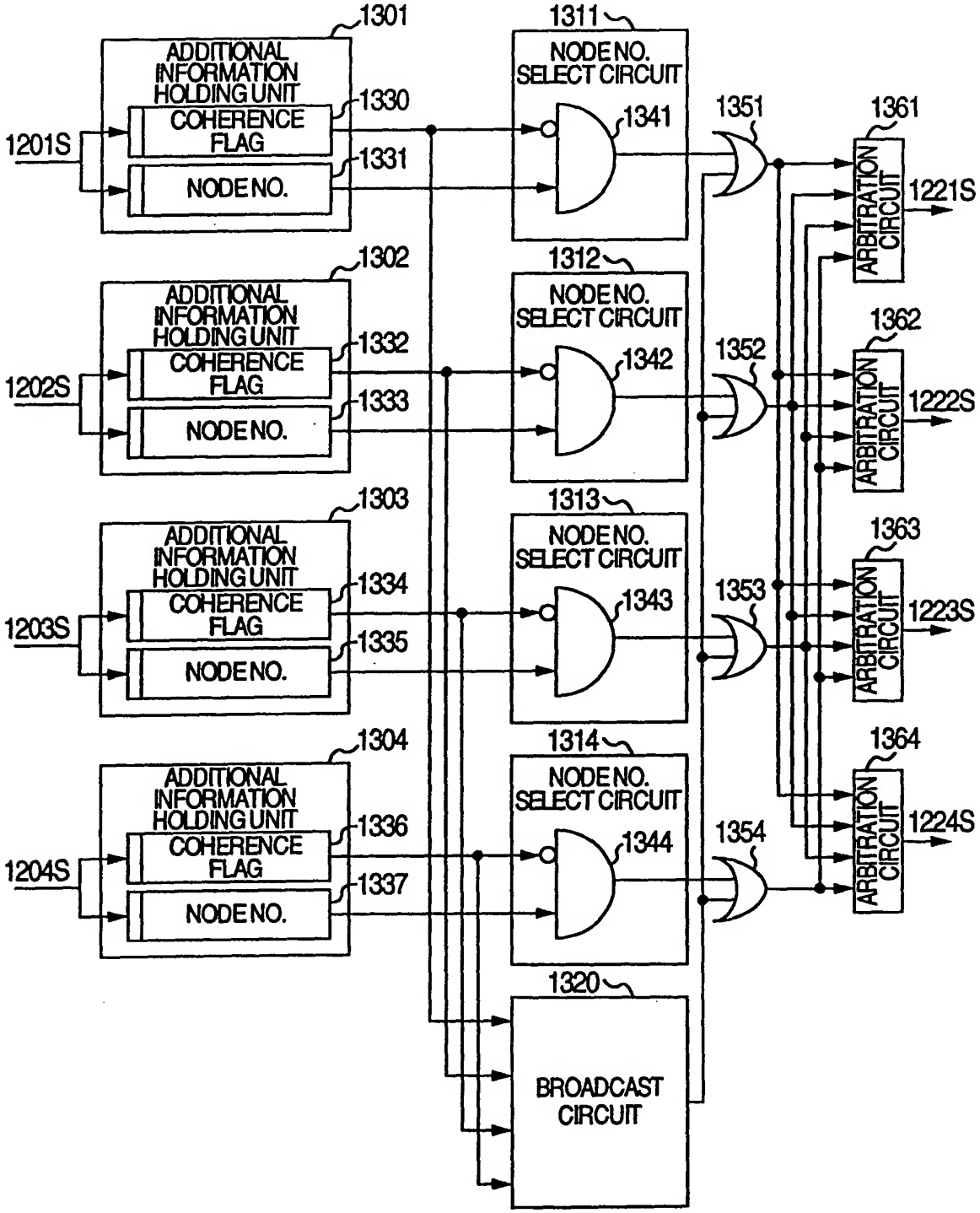

1201
1221
1231
NODE 101
INPUT BUFFER
SELECTOR
OUTPUT BUFFER
NODE 101
1202
1222
1232
NODE 102
INPUT BUFFER
SELECTOR
OUTPUT BUFFER
NODE 102
1203
1223
1233
NODE 103
INPUT BUFFER
SELECTOR
OUTPUT BUFFER
NODE 103
1204
1224
1234
NODE 104
INPUT BUFFER
SELECTOR
OUTPUT BUFFER
NODE 104
1300
1201S
1202S
1203S
1204S
ROUTE DESIGNATION CIRCUIT
ADDITIONAL INFORMATION HOLDING UNIT
NODE NO. SELECT CIRCUIT
BROADCAST CIRCUIT
1221S
1222S
1223S
1224S
1301 TO 1304
1311 TO 1314
1320

FIG. 13


1301
ADDITIONAL INFORMATION HOLDING UNIT
COHERENCE FLAG
NODE NO.
1330
1331
1201S
1311
NODE NO. SELECT CIRCUIT
1341
1351
1361
ARBITRATION CIRCUIT
1221S
1302
ADDITIONAL INFORMATION HOLDING UNIT
COHERENCE FLAG
NODE NO.
1332
1333
1202S
1312
NODE NO. SELECT CIRCUIT
1342
1352
1362
ARBITRATION CIRCUIT
1222S
1303
ADDITIONAL INFORMATION HOLDING UNIT
COHERENCE FLAG
NODE NO.
1334
1335
1203S
1313
NODE NO. SELECT CIRCUIT
1343
1353
1363
ARBITRATION CIRCUIT
1223S
1304
ADDITIONAL INFORMATION HOLDING UNIT
COHERENCE FLAG
NODE NO.
1336
1337
1204S
1314
NODE NO. SELECT CIRCUIT
1344
1354
1364
ARBITRATION CIRCUIT
1224S
1320
BROADCAST CIRCUIT